REMARKS/ARGUMENTS

I. Introduction

Applicants graciously thank the Examiner for calling their representatives to withdraw all the rejections from the Office Action after having read a faxed, draft response in preparation for a scheduled interview. The following below details Applicants' response to the Office Action.

A. Status of Claims

- Claims 1-16 remain in this application.
- Claims 1 and 10 are the only independent claims under review.
- Claims 1-8 and 10-15 stand rejected under 35 U.S.C. § 102(e).
- Claims 9 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over **Matsunaga** et al., U.S. pat. No. 5,440,675.

B. Phone Summary

Applicants appreciate and graciously thank the Examiner for extending courtesy to the Applicants and their representatives' request for an interview. Examiner granted an interview for Tuesday, August 10, 2004. Applicants faxed a draft response to the Office Action to the Examiner for review. Having read the draft response, Examiner telephoned Applicants' representatives on Friday, August 6, 2004 to inform Applicants that Examiner is withdrawing all the rejections from the Office Action. Examiner further indicated that the withdrawal will be written formally after Applicants formally file a response.

II. Claims

A. Rejections under 35 U.S.C. § 102(e) are improper.

1. Rejecting Independent Claims 1 and 10 is improper.

The rejections to Independent Claims 1 and 10 are improper because **Matsunaga** does not disclose at least an ordering relation, goals or lattice. See, e.g., Claim 1, p. 19 ("applying said ordering relation to said plurality of goals to create a lattice").

a. Ordering relation is not anticipated.

Upon reviewing **Matsunaga**'s steps, Applicants do not believe **Matsunaga** incorporates the concept of "ordering relation." The Examiner does not specifically identify where **Matsunaga** discloses this

concept. Applicants believe the closest **Matsunaga** comes to "ordering relation" is using the terms "assembling order." However, "assembling order" refers to a different concept.

Matsunaga primarily focuses on analyzing an object expressed through a network constituting nodes and branches, as well as the weight of the branches, for the allocation and scheduling of resources. See **Matsunaga**, col. 1, lines 11-16; col. 2, lines 13-22. The nodes to be processed to determine the weight of the branches are classified in patterns in the resource allocation, scheduling and analysis of maximum flow. Id. at col. 3, lines 61-66. This process can be carried out in the order of procedures proportionally to the total number of branches. Id.

Apparently, **Matsunaga**'s assembling order refers to the way branches (sometimes referred to as arcs in **Matsunaga**), are aligned. This order is "constituted wiring," connecting nodes and other components of an apparatus. See **Matsunaga**, col. 10, lines 43-45, 64-66.

In contrast, the present invention discloses the concept of "ordering relation" by defining the concept as "any property that can be said to hold (or not to hold) for two objects in a specified order such that $x<y$, $y<x$, or x and y are unrelated (where '<' means 'included in')." See Specification, p. 4, 13-27. "An ordering relation is used as a means of classifying the multiplicity of goals as (a) included goals (i.e., goals which are included in, are a part of, or contribute to the accomplishment of, high-level goals), (b) including goals (higher-level goals which encompass 'included goals'), and (c) unrelated goals." Id. at p. 4, line 30 – p. 5, line 2. An included goal, as defined in the present invention, is "one which is comprised of included goals, i.e., included goals are 'included' in an included goal." Id. at p. 5, lines 4-5.

In sum, **Matsunaga** applies a different concept compared to that of the present invention. On one hand, **Matsunaga**'s "assembling order" concept refers to how components are connected (e.g., assembled). On the other hand, the ordering relation in the present invention simply refers to what goals are included, for example, in a decision-making process.

b. Matsunaga does not teach a goal lattice.

Upon further review of **Matsunaga**'s steps, Applicants do not believe **Matsunaga** incorporates a goal lattice. **Matsunaga** discloses a "linear programming model of a graph." See **Matsunaga**, Claim 1, col. 13, line 45. In contrast, the goal lattice in the present invention is a

"lattice" with a precise mathematical definition, which is not a linear programming model of a graph.

A goal lattice is defined in the present invention as the lattice and the values assigned to each of the goals of the lattice. See Specification, p. 5, lines 25-27. A lattice is defined as "a representation of the relationship among all the goals as imposed by the ordering relation, preferably having a greatest lowest bound and a least upper bound." Id. at lines 11-13. The values assigned to goals are used ". . . to determine the relative values of specific sensor actions in terms of how they contribute to goals . . . ." See Specification, p. 17, lines 18-20. Using these values ". . . allows for a partitioning and subsequent independent optimization of the sensor scheduling task from the sensor management task." Id. at lines 20-21.

The goal lattice may be created by identifying all relevant goals, creating a lattice from an ordering relation and for each layer in the lattice, apportioning each goal's values among directly included goals and accruing values at each included goal. See Specification, p. 5, lines 11, 25-26; p. 11, lines 3-6.

Having a goal lattice permits one ". . . to quantify and make measurable amorphous, non-measurable, 'soft' goals", which are goals that are not directly quantifiable. See Specification, p. 12, line 20; p. 15, lines 15-16. "It not only allows for the straightforward apportionment of goal values from soft goals to specific action items, but forces the system designer to formally describe the goals of the system, as well as to quantify the interrelationship among system goals." Id. at p. 15, lines 16-19. Moreover, "[r]ather than defining the system in terms of how it behaves against specific environmental scenarios, or engineering performance measures which are indirect measures of the accomplishment of system goals, the system can now be designed in terms of goal accomplishment." Id. at p. 15, line 19 – p. 16, line 2. "Since this is a goal directed system, if the goals have been enumerated correctly and their interrelationship properly specified, no system can perform better, because goal achievement is the performance measure." Id. at p. 16, lines 7-9.

Applicants believe that this design clearly distinguishes the present invention from **Matsunaga**. By virtue of having a linear programming model of a graph, **Matsunaga**'s graph is unidirectional and not a goal lattice. As such, values flow and are modified by an iterative method. But, there is no accrual of values. This accrual of values is an enhancement of the concept of a lattice and is neither a part of **Matsunaga**'s graph nor the definition of a lattice.

Additionally, **Matsunaga** discloses a concept of nodes in its linear programming model. According to **Matsunaga**, nodes represent the status and branches representing the status transition. See **Matsunaga**, Claim 1, col. 13, lines 46-47. The closest term, in the present invention, to "node" is "goal." However, "goal" is different from "node" in the sense that "goal" means "any task, activity, end-result, etc., which is to be considered in order to accomplish the system objective." See Specification, p. 3, line 32 – p. 4, line 1. For example, in a business setting, goals can include, e.g., opening a new store, purchasing land for the new store, hiring contractors to build the new store, etc. Id. p. 4, lines 1-8. In essence, **Matsunaga**'s "nodes" are different creatures compared to the present invention's "goals."

Furthermore, **Matsunaga** includes at least one closed loop. See **Matsunaga**, Claim 1, col. 13, lines 47-48. The present invention is clearly distinguishable from **Matsunaga** because the present invention involves a goal lattice. Because a lattice cannot have a closed loop, the present invention cannot have a closed loop.

Because Applicants believe **Matsunaga** does not disclose an ordering relation as defined in the present invention or a goal lattice, **Matsunaga** does not teach the same invention. Hence, Applicants respectfully request the withdrawal of these rejections for Independent Claims 1 and 10.

2. Rejecting Dependent Claims 2-9 and 11-16 should be overcome.

Applicants believe the above response overcomes **Matsunaga** with respect to Independent Claims 1 and 10, the rejections to Dependent Claims 2-9 and 11-16 are now improper. These dependent claims are dependent upon the independent claims and include all of the limitations of the independent claims. Thus, Applicants respectfully request the withdrawal of the rejections to these dependent claims.

B. Rejection under 35 U.S.C. § 103 should be overcome.

The rejection of Claims 9 and 16 under 35 U.S.C. § 103(a), is currently rejected as being unpatentable over **Matsunaga** et al., U.S. pat. No. 5,440,675.

Applicants believe that the response in section II.A.1 overcomes **Matsunaga**, and thus Independent Claims 1 and 10 are now in condition for allowance. Because Claim 9 depends on Independent Claim 1 and includes all the limitations of Independent Claim 1, Dependent Claim 9 is also now in condition for allowance and thus overcomes the obviousness rejection. In addition, because Claim 16 depends on Independent Claim 10 and includes all the

limitations of Independent Claim 10, Dependent Claim 16 is also now in condition for allowance and thus overcomes the obviousness rejection. Thus, Applicants respectfully request the Examiner to remove the 35 U.S.C. § 103 rejection on Dependent Claims 9 and 16.

C. The remaining prior art references of record do not anticipate the present application.

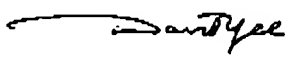
Applicants also thank the Examiner for his consideration of **Lobley** et al., U.S. pat. No. 5,758,026, **Yufik** et al., U.S. pat No. 5,794,224, and **Peterson** et al., U.S. pat No. 6,327,551. However, Applicants believe that like **Matsunaga**, these references do not anticipate the present invention.

III. Conclusion

For all of the reasons advanced above, Applicants respectfully assert that the application is in condition for allowance and, thus, respectfully solicit an action of allowance. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' agents at the telephone number shown below.

In the event that an extension of time is required, or may be required in addition to that requested in a petition for an extension for time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to Deposit Account No. 501450.

Respectfully submitted,



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